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SEMI Standards Enable Remote Fab Operation And SEMI Memory Developments

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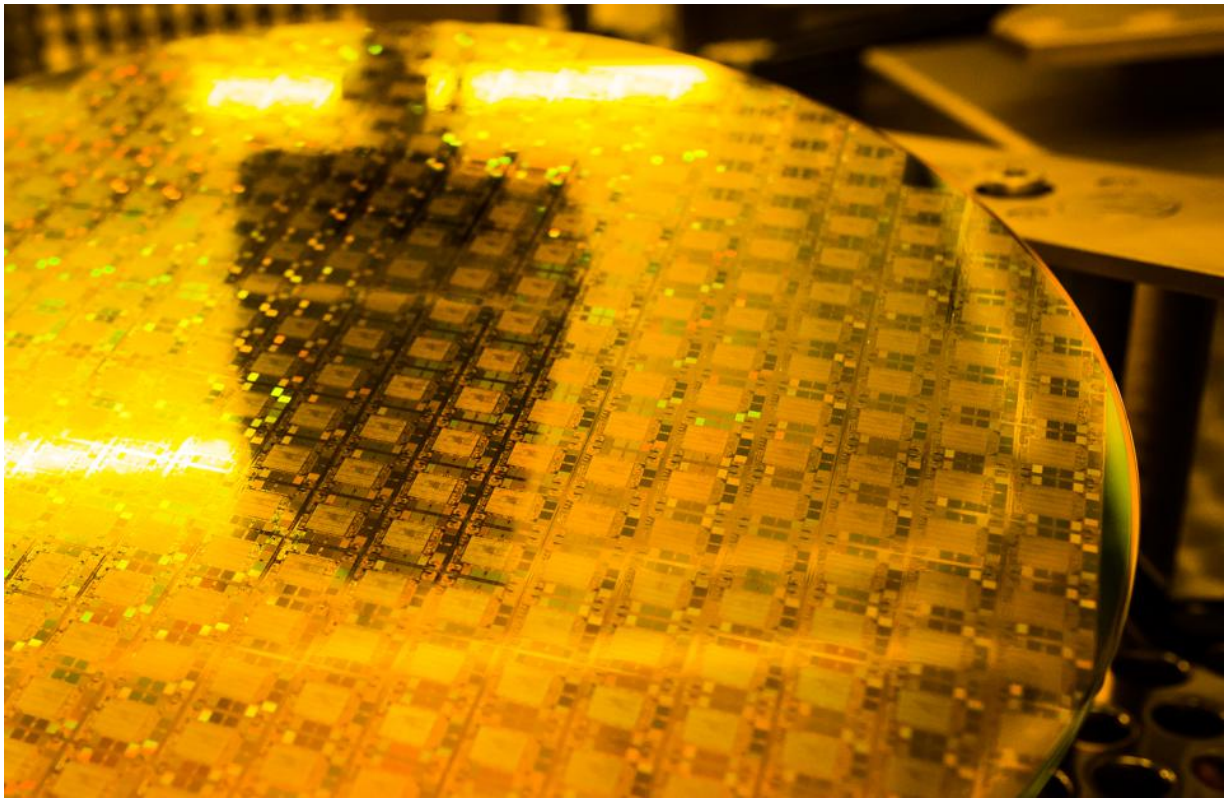
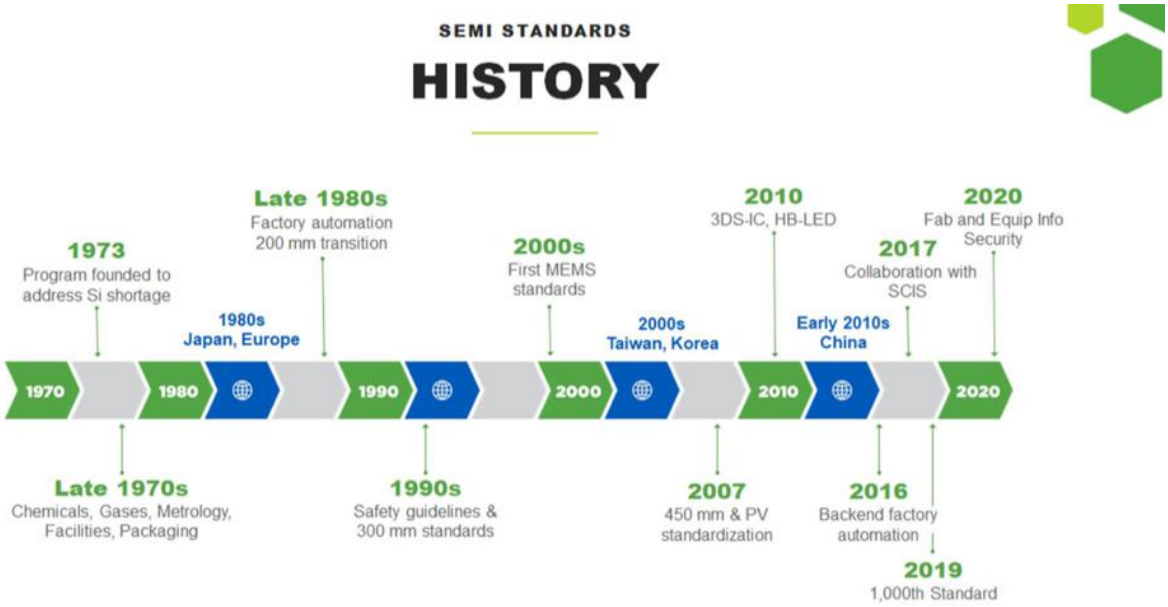


A semiconductor in a wafer fab semiconductor plant Photo: Christoph Schmidt/dpa (Photo by Christoph ... [+] PICTURE ALLIANCE VIA GETTY IMAGES

uring the 2020 Virtual SEMICON West, SEMI talked about the role of its standards and emerging cybersecurity developments to enable continued operation of semiconductor manufacturers during the Covid-19

pandemic. These standards provide a foundation for factory automation and thus are making it possible for thousands of tech staff to keep working during the current and possible future shutdowns. During the pandemic shutdown chip manufacturer employees were able to use tablets and virtual reality headsets or goggles to do work that once required traveling engineers. The figure below shows the history of SEMI standards.



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James Amano, senior director of International Standards for SEMI said that between February and April 2020, the use of software for remote diagnosis and management of semiconductor manufacturing tools by semiconductor suppliers more than doubled, and usage remained at record-high levels in May and June. He said that with the groundwork established by standards, a lot of technicians have continued to handle vital diagnostics and control, but from home.

Continued SEMI standards development efforts should enable safe remote management of semiconductor fabs. These efforts include SEMI draft document 6566 (led by Intel and Cimetrix) on malware-free equipment integration and SEMI Draft Document 6506, Specification for cybersecurity of FAB equipment.

During the 2020 Virtual SEMICON there were talks from Micron on DRAM developments and some mention of MRAM by Applied Materials.

Thy Tran, from Micron spoke about how the industry is working to achieve more-dense DRAM. She mentioned that as it gets harder to shrink memory bits there is more focus on increasing periphery scaling and the pitch cell. High k metal gates help on the pitch cell scaling. Periphery CMOS lags behind logic technology by about a decade and cost effectively bridging this gap is a priority. DRAM interconnect scaling is another important factor and requires pitch multiplication or the use of EUV.

On lithography beyond the 1-beta node EUV can provide a cost reduction opportunity (less steps and complexity required). Lower cell capacitance requires lower drive but loses sense margin, perhaps requiring more frequent refreshes and greater possible wordline disturbs. These are just a few of the technical issues that have slowed the capacity density growth of mainstream DRAM technology. Following is the summary from her talk: cost may be beneficial beyond 1-beta node, longer word-lines and bit-line to maximize array efficiency saturation with array scaling is a challenge, more aggressive CMOS and interconnect scaling needed as cell shrink slows down, process and tool advances require every node to extend scaling path and process design points and uniformity control are critical to enable process margins.

Ellie Yieh from Applied Materials talked about replacing DRAM and SRAM with MRAM to save power in embedded devices during a SEMICON panel discussion. The MRAM technology has future generations that will continue

to reduce MRAM device power, including voltage controlled MRAM (VCM). There are also developments by Chinese NAND flash and DRAM companies, mostly announced at the Shanghai SEMICON that provide some insights on memory developments in China.

At SEMICON China in Shanghai, Yangtze Memory said that it was making 64-layer NAND in Q4 2019 and said it had developed 128-layer devices in April, 2020. Yangtze Memory started work on a 300,000 wafers per month, $24B NAND plant in Wuhan, which the company says would be able to supply 23% of the current world market. By the end of 2021 the company is expected to have a capacity of 80,000 wafers per month. It is likely that the first customers for Yangtze products will be for internal Chinese products.

Changxin Storage (CXMT) is a Chinese DRAM manufacturer. At the end of February 2020, the company announced DDR4 memory chips, DDR memory sticks and LPDDR4 memory chips. Chinese DIMM products using these memories are now available in China and ADATA Technology, one of the leading memory brands said that it will use CXMT memory in its DIMM products. Based upon a TechInsights presentation at the Shanghai SEMICON the bit density of the CXMT DRAM products corresponds to a 24nm process.

SEMICON West showed how standards have been used to keep semiconductor manufacturing ongoing even with employees working remotely. Micron spoke about challenges for denser DRAM and Applied Materials talked about advantages of MRAM . SEMICON Shanghai gave insights on memory developments in China.